REMARKS

Applicant notes with appreciation the indication by the Examiner of allowable subject matter recited in Claims 2, 3, 4, 11, 12, 14, 15, and 18-23. Claims 1-23, of which Claims 1, 6, 9, and 18 are independent, are now pending in the application.

Rejection under U.S.C. § 102

The Office Action rejects Claims 1, 5-10, 13, 16, and 17 as being anticipated by U.S. Patent No. 5,917,364 of Nakamura (hereinafter "Nakamura"). Applicant respectfully traverses this rejection on the basis of the following arguments, and further contends that Nakamura fails to disclose all elements of these claims, as described below, and hence does not anticipate the claimed invention.

For purposes of clarity in the discussion below, the respective claim rejections under 35 U.S.C. § 102 are discussed separately.

A. Rejection of Claims 1 and 5 under 35 U.S.C. § 102(b):

The Office Action rejects Claims 1 and 5 as being anticipated by Nakamura. Applicant respectfully traverses this rejection on the basis of the following arguments and further contends that Nakamura fails to disclose all elements of these claims, as described below and hence, does not anticipate the claimed invention.

Nakamura is directed to a bi-directional interface circuit for reducing simultaneous switching noise and power consumption even when transitions of a signal direction occur. The bi-directional interface circuit of Nakamura includes an encoder for generating an output bit sequence in synchronization with a clock cycle of the bus lines of the interface circuit. The output bit sequence generated by the encoder is in a low weight code format so that a signal alteration rate of the output bit sequence as compared to a preceding bit sequence transmitted on the bus lines is less than half. The object of Nakamura is to encode data on a *single ended* input into coded data on a *single ended* output to reduce noise and power consumption of integrated circuits.

Applicant's inventions recited in Claims 1 and 5 are directed to a logic circuit to perform an XOR logic function without the logic circuit entering an unstable state. The logic circuit includes an input circuit and an output circuit. The input circuit converts a number of static input signals to a number of complimentary dual rail domino output signals having one or more valid states. The output circuit performs a number of the XOR logic functions on the complimentary dual rail domino output signals without the logic circuit entering an unstable state. Consequently, the logic circuits of Claims 1 and 5 are well suited for use to generate a "finish" signal, which, in turn, can be used to start evaluation of the next stage in a data pipeline without the need for additional circuitry to gate or delay the finish signal to prevent a false start.

The inventions recited in Claims 1 and 5 distinguish patentability over the Nakamura patent. The Nakamura patent does not disclose a logic circuit to perform a XOR logic function without the circuit entering an unstable state. Furthermore, the Nakamura patent fails to disclose that the logic circuit includes an input circuit to convert a plurality of static input signals to a plurality of complimentary dual rail domino output signals having one or more valid states. That is, Nakamuramerely encodes a *single ended* input signal into a coded *single ended* output signal.

In contrast, Claims 1 and 5 each recite a logic circuit to perform a XOR logic function without the logic circuit entering an unstable state. As such, the logic circuit of Claims 1 and 5 includes an input circuit to convert a number of static input signals to a number of complimentary dual-rail domino output signals having one or more valid states. Nowhere does the Nakamura patent disclose conversion of a static input signal to a complimentary dual rail domino output signal having one or more valid states. The interface circuit of Nakamura merely receives a single ended input signal and outputs the same.

Accordingly, the Nakamura patent does not anticipate Claims 1 and 5. As such, Applicant requests the Examiner to reconsider and withdraw the rejection of Claims 1 and 5 under 35 U.S.C § 102(b).

B. Rejection of Claims 6-8 under 35 U.S.C. § 102(b):

The Office Action rejects Claims 6-8 as being anticipated by Nakamura. Applicant respectfully traverses this rejection on the basis of the following arguments, and further contends that Nakamura fails to disclose all elements of these claims, as described below and hence, does not anticipate the claimed invention.

The inventions recited in Claims 6-8 distinguish patentability over the Nakamura patent. The Nakamura patent is concerned with reducing noise at an interference caused by bits in a bus transitioning between states. Nakamura does not disclose a method for performing a near simultaneous comparison of multiple bits using a logical XOR function in a manner that avoids the XOR function hazard of the logical XOR function. Furthermore, the Nakamura patent fails to disclose that the method includes a step of generating a plurality of dual rail domino output signals from a plurality of input signals in a manner that avoids an unstable state in a logical XOR circuit to avoid the XOR function hazard in the logical XOR circuit.

In contrast, Claims 6-8 each recite a method for performing a near simultaneous comparison of multiple bits using a logical XOR function in a manner that avoids an XOR function hazard of the logical XOR function. The method of Claims 6-8 avoid what is known in the art as a "function hazard" in part by generating a number of dual rail domino signals from a number of input signals in a manner that avoids an unstable state in a logical XOR circuit to avoid the XOR function hazard in the logical XOR circuit. Nowhere does Nakamura disclose such a feature. Nakamura is merely concerned with single ended or single rail signaling.

Accordingly, Claims 6-8 are not anticipated by the Nakamura patent. Applicant requests the Examiner to reconsider and withdraw the rejection of Claims 6-8 under 35 U.S.C. § 102(b).

C. Rejection of Claims 9, 10, 13, 16, and 17 under 35 U.S.C. § 102(b):

The Office Action rejects Claims 9, 10, 13, 16, and 17 as being anticipated by Nakamura. Applicant respectfully traverses this rejection on the basis of the following arguments, and further contends that Nakamura fails to disclose all elements of these claims, as described below and hence, does not anticipate the claimed invention.

The inventions recited in Claims 9, 10, 13, 16, and 17 distinguish patentability over the Nakamura patent. The Nakamura patent does not disclose a circuit to perform a substantially simultaneous comparison of multiple bits that includes an encoder circuit and a XOR logic circuit not subject to the XOR function hazard to perform the substantially simultaneous comparison of multiple bits. The encoder circuit receives a number of input signals and generates a number of dual rail domino output signals from the input signals in a manner that prevents each of the dual rail domino output signals from entering an invalid state. The XOR logic circuit performs the substantially simultaneous comparison of multiple bits on the dual rail domino output signals from the encoder circuit. The interface circuit of Nakamura, in contrast, does not generate a plurality of dual rail domino output signals from a plurality of input signals and further fails to disclose a XOR logic circuit not subject to the XOR "function hazard" to perform a substantially simultaneous comparison of multiple bits in the dual rail domino output signals from the encoder circuit.

In contrast, Claims 9, 10, 13, 16, and 17 each recite a circuit to perform a substantially simultaneous comparison of multiple bits that includes an encoder to generate a number of dual rail domino output signals from a number of input signals in a manner that prevents each of the dual rail domino output signals from entering an invalid state. The circuits also includes a XOR logic circuit not subject to the XOR "function hazard" to perform the substantially simultaneous comparison of multiple bits on the dual rail domino output signals from the encoder circuit. As such, the circuits recited in Claims 9, 10, 13, 16, and 17 are able to perform a substantially simultaneous comparison of multiple bits and avoid the XOR "function hazard" of the XOR logical function. The Nakamura patent fails to disclose that the interface circuit generates dual rail domino output signals from input signals

in a manner that prevents each of the dual rail domino output signals from entering an invalid state.

Thus, Claims 9, 10, 13, 16, and 17 are not anticipated by the Nakamura patent. Accordingly, Applicant requests the Examiner to reconsider and withdraw the rejection of Claims 9, 10, 13, 16, and 17 under 35 U.S.C. § 102(b).

CONCLUSION

It is believed that the claims in their current form distinguish over the cited references. Should the examiner feel that a telephone conference with Applicant's attorney would expedite prosecution of this application, the Examiner is urged to contact the Applicant's attorney at (617) 227-7400.

Respectfully submitted,

LAHIVE & COCKFIELD, LLP

David R. Burns

David R. Burns, Esq.
Registration No. 46,590
Attorney for Applicants

28 State Street
Boston, MA 02109
(617) 227-7400

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